Attorney Docket No. 20040144.ORI

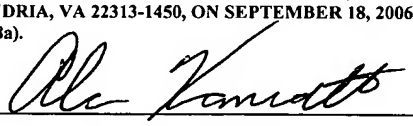
Client Docket No. CFP00353

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re App	:	Herng-Jer Lee et al.	:	Examiner James C. Kerveros
Serial No.	:	10/827,507	:	Art Unit 2138
Filed	:	April 19, 2004	:	Confirmation No. 3480
For	:	Method of Scan Chain Reordering for Lowering VLSI Power Consumption		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I CERTIFY THAT THIS PAPER IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE AS FIRST CLASS MAIL WITH SUFFICIENT POSTAGE AND IS ADDRESSED TO THE COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, ON SEPTEMBER 18, 2006 (37 C.F.R. 1.8a).



AMENDMENT

Dear Sir:

In response to the Office communication mailed April 17, 2006, please amend the above application as follows: